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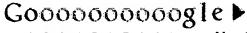
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involved the choice of either 2-wide or 4-wide **32bit** floating-point data parallel computations. This
The basic approach was to double-cycle existing **64-bit** hardware. The performance benefit of selecting
Passing parameters would either require more **conversion** instructions or would be through memory, as
developer.intel.com/technology/itj/q21999/articles/../pdf/simd_ext.pdf

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in parallel on four 16-bit data types or on two **32-bit** data types (for more detail see the sidebar,
the entire width of a processor data path (32 or **64 bits**)even when processing the small native data
executions for arithmetic operations, data **conversion**, and rearrangement operations. Subword versions
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hardware, and up to 4 Mbytes of memory. There is a **32-bit** wide data path between each processing unit and
node is composed of 32 one-bit processors and one **64-bit** floating-point accelerator, a routing chip and
.11 4.2. Fortran 77 to Fortran 90 **conversion** .12 5.
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point register file, sharing the **64-bit** and **32-bit** floating point registers. The Graphics Status
the floating point register file, sharing the **64-bit** and **32-bit** floating point registers. The Graphics
bytes or 16-bit words) within a wide (typically **64-bit**) data word on modern microprocessors. Other
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Report on the AES Candidates - Baudron, Gilbert, Granboulan.. (1999) (Correct) (6 citations)
be based on **64-bit** architectures rather than on **32-bit** ones. Microprocessor manufacturers are currently
believe that future technologies will be based on **64-bit** architectures rather than on **32-bit** ones.
most microprocessors already have some endianess **conversion** routines #BSWAP for Intel #which cost little
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the information about Hamming weight of certain **32-bit** words produced in the process of decoding m by
The padding consists of bit 1, 71 zero bits and a **64-bit** representation of the message bit length. The
section 3 we present a very simple but efficient **conversion** of the Manger/Bleichenbacher breaking oracle to
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a PCI bus interface that can be operated in either **32 bit** or **64 bit** mode (the PE board uses it in **32 bit**
line cards. Such cards can use either a 16 bit or **32 bit** Utopia interface, although some (including
interface that can be operated in either **32 bit** or **64 bit** mode (the PE board uses it in **32 bit** mode)The
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for the ALUs or functional units is less than **32 bits**. Some of the ALUs are the split-ALUs which can
2 (Alus) Bar(18 Gb/s) Nec Risc Core A Simd 32/ **64-Bit** Bus 16 2.0 600 [19] V830r/av(Coprocessor 64(
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1 January 1900. The integer part is in the first **32 bits** and the fraction part in the last **32 bits**, as
and Formats NTP timestamps are represented as a **64-bit** fixed-point number, in seconds relative to 0000
convenient multiple-precision arithmetic and **conversion** to Time Protocol representation (seconds)but
www.tzi.de/~cabo/pdfrfc/rfc958.txt.pdf

Time Stamp Counters Library - Measurements with Nano Seconds .. - Etsion, Feitelson (2000) (Correct) (1 citation)
that is supported by the Intel hardware is only **32 bits** in size. Some compilers support **64 bit** integral
2.1 Types The hardware's time stamp counter is a **64 bit** integral register. Currently, the biggest
represent all **64 bit** integer values, and since **conversion** to and from it incur unnecessary overhread, we
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to the early seventies, what could be done with **32 bits** was already quite clear nowadays, we still see
register size expansion is slow: 4 bits in 1971, **64 bits** in 1998 1 The register and logical
over a bunch of registers this implies some **conversion** stages that may be rather slow. This problem is
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up to 256 bits (with increment by a multiple of **32 bits**) by iterating a fully parallelizable round
such as software implementations on 8-bit, 16-bit, **32-bit** and **64-bit** microprocessors and a dedicated
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common implementations take advantage of the 8 or **32-bit** host CPU to externally execute the work 2 we
most e#orts focused on conventional 8, 16, 32 or **64-bit** architectures (we refer the reader to [7, 1, 2]
Radix/Modular and Modular/Radix representation **conversions**. The next section sheds light on these
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Table Lookup Structures for Multiplicative Inverses Modulo 2 - David Matula Alex (Correct)
employing Equation 1 would be needed to obtain a **32-bit** integer modular inverse. Just two iterations
for providing a seed inverse for obtaining 32/**64-bit** multiplicative inverses by one/two iterations of
essentially a "discrete log triple transform"**Conversion** between standard binary and Benschop's exponent
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yield short integer values actually leave an I4 (32bit) value on the stack, but it is guaranteed that
arithmetic is available and efficient on current **64 bit** hardware. For this reason, numeric instructions
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